Datasheet F3200E

Thirty-two Channel High-Speed Current Digitizer

Features

- Thirty-two parallel multi-range current to voltage converter channels
- Bipolar inputs, bandwidth DC to 250 kHz
- Dynamic range <1 nA to 10 mA over four measurement ranges
- Thirty-two 14 bit 1 MHz ADCs for fully parallel sampling; digital downsampling to increase effective resolution
- Integrated data buffering and communications
- Multiple digital filtering options
- Data acquisition can synchronize to an incoming trigger, or the F3200E can provide a trigger to external devices
- Integrated high-precision calibration test sources covering all ranges
- Optional integrated HV supply with loopback validation
- General-purpose analog and digital interface
- Actuator solenoid control interface
- Ethernet, fiber-optic or serial communications interfaces
- Diagnostic control software program included
- IG2 interface software for connection to EPICS and related programs

Applications	• Faraday cup arrays • Swept beam systems • Multi-segment photodiode arrays • Multi-electrode ionization chambers • Low-current measurement with good time resolution
Options	• Auxiliary HV output for detector bias • Current limiting input resistors

Specifications

Operating principle	Multi-range I-V converters on every channel each with anti-alias low-pass filtering and individual successive approximation bipolar ADCs.
Signal inputs	2 x 16 inputs on DB25 female connectors
Current ranges	+/-10 mA, +/-1 mA, +/-100 µA, +/-10 µA, software selectable Current ranges can be set in groups of four channels.
Input impedance	< 40 ohm
Input protection	Back to back fast diode pair; optional current limiting series resistor
Noise (unloaded)	< 0.1% of full scale rms noise for 10 mA, 1 mA, 100 µA, 10 µA ranges, for a single conversion acquisition. Improves by 1/√N where N is number of conversions averaged into each sample, to a minimum of 0.001% of full scale.
External accuracy	Readings within +/- (0.1% of nominal reading + 0.1% of full scale) after calibration, relative to a traceable external standard current source.
Analog bandwidth	Anti-aliasing filter DC to 250 kHz (-3dB) with four-pole filter.
Linearity	Deviation from best fit line of individual readings < 0.1% of full scale.
Internal calibration currents	8.333 (+/- 0.003) mA (10 mA range) 833.3 (+/- 0.3) µA (1 mA range) 83.33 (+/- 0.03) µA (100 µA range) 8.333 (+/- 0.003) µA (10 µA range) Used by automated internal calibration routine to obtain gain and offset for each channel on each range.
Calibration source drift	< 3 ppm / C
Measurement drift	< 0.5% over 12 hours (environment 20 +/-2 C).

Digitization	Thirty-two ADCs, 14 bit bipolar, 1 MHz Effective digitization increased by on-board averaging.
Simultaneity	All ADCs convert together to within 20 nsec.
Data capture	32 channels converted and transferred to local memory in < 500 nsec.
Digital filtering	Averaging 1 to 65000 ADC conversions (downsampling). Averaging counters 32 bit depth.
Local data buffer	Up to 2000 x 32 channels in burst mode Up to 1000 x 32 channels in sweep mode.

Specifications (continued)

Acquisition modes	Internal (free running and continuous transfer to host) Burst mode (on-board buffering of contiguous blocks of readings). Sweep mode (on-board buffering of triggered acquisitions, averaging across multiple sweeps. Oscilloscope style).

Gates (triggering)	
External Gate input	0 / +5 V (TTL level), 10 kohm input impedance.
External Gate output	0 / +5 V (TTL level), able to drive 50 ohm load. Gate in/out latency < 50 nsec.
General purpose I/O	
Analog outputs	Three, +/-10V, 10 mA compliance. 16 bit resolution, low transition glitch energy. Maximum update rate 250 kHz.
Analog inputs	Four, +/-10V, two-pole analog low pass filter 17 kHz. 16 bit resolution, maximum conversion rate 400 kHz.
Digital outputs	Four, TTL levels, 5 mA typical, 35 mA maximum (single output)
Digital inputs	Four, TTL levels. 50 kohm pull up to +5VD.
User voltages	One +24 VDC out 130 mA fused. One +5 VDC out 200 mA fused.
Actuator control	
Switched 24 VDC	One, relay switched. 130 mA fused. Also configurable as a voltage-free contact closure as a build time option.
Switched 5 VDC	One, relay switched. 130 mA fused. One FET switched, internal 10 kohm pull-up to 5 V.
Limit switch inputs	Two. Opto-isolated, 10 kohm current limiting resistor, returned to 24 V return.
Fiber optics	
Configuration	Four transmitters, two receivers. Arranged as two transmitter/receiver communication pairs plus two uncommitted digital outputs.
High voltage option	
HV PSU	0 to 2000 V / 1000 V / 500 V / 200 V programmable, (range and polarity build-time options). 1 watt max. Noise and ripple < 0.1%.
HV monitoring	Independent voltage dividers on output and loopback input.

Specifications (continued)

Power input	+24V (+/- 2V) DC, 750 mA typ, 1200 mA max. excluding load on actuator port.
Controls	Two rotary switches for loop address and comms mode/baud rate. One push button for processor reset.
Displays	Front panel: Illuminated logo for power on; “HV on” LED. Rear panel: Dual quad LED banks (power, device status, comms activity, comms mode)
Case	1U 19” x 250 mm deep steel chassis with Al alloy front panel, IP43. Fan cooled.
Weight	2.8 kg (6.2 lb)
Operating environment	10 to 35 C (15 to 25 C recommended to reduce drift and offset) , < 70% humidity, non-condensing, vibration < 0.1g all axes (1 to 100 Hz)
Shipping and storage environment	-10 to 50 C, < 80% humidity, non-condensing, vibration < 2g all axes, 1 to 100 Hz

Interfacing

Interfaces	Ethernet 10/100, UDP and TCP/IP. Auto MDIX switching.
	RS-232 / 485 8 bit binary. Selectable baud rate.
	Fiber-optic loops, Two, 10 Mbit/sec serial, 9-bit asynchronous binary. The F3200E can act as a loop controller or a looped slave device.

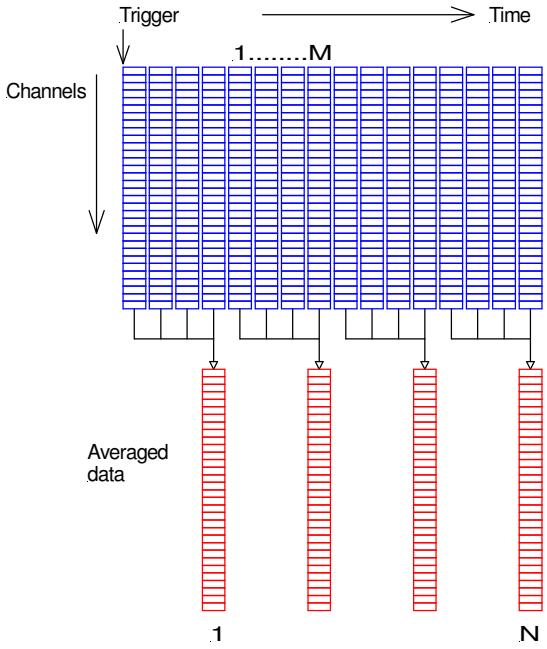
Host computer	PTC DiagnosticG2 host program supplied for Windows or Linux PC. IG2 interface software allowing connection to EPICS data distribution, and therefore supported hosts environments including C++, C#, Labview ™, Matlab ™, Python.

Averaging modes

Burst mode

For bandwidth reduction when non-repetitive signals are noisy. Time resolution is reduced according to the amount of averaging.

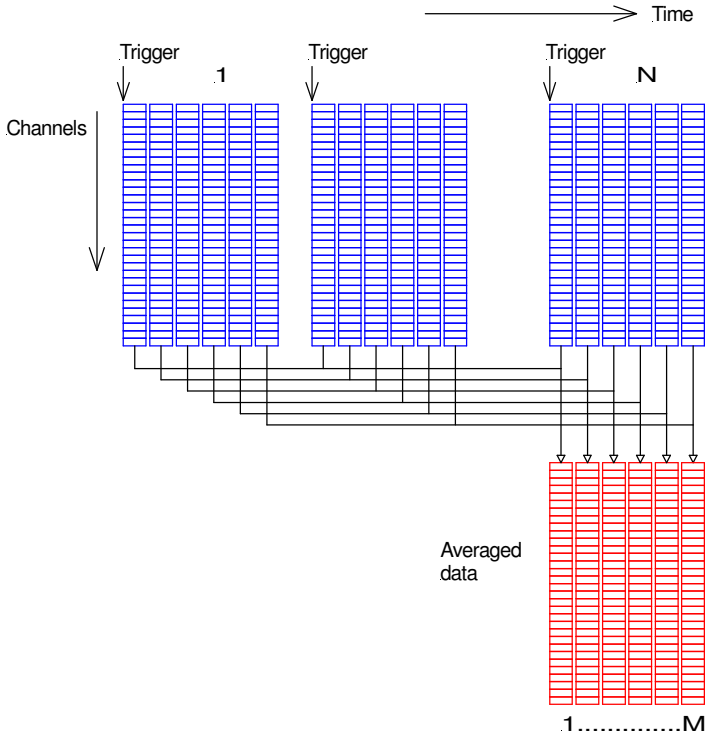
Groups of M conversions (32 channels), 1 <= M <= 65535, are averaged (downsampled) to give a set of N readings (32 channels), 1 <= N < (no limit)



Sweep mode

For bandwidth reduction where signals are repetitive. Time resolution is preserved.

Groups of M conversions (32 channels), 1 <= M <= 1000, are averaged across N triggers, 1 <= N <= 65535



Connectors

Signal inputs — Two DB25 female, front panel. Channels 1-16, channels 17-32.

1	In 02 (In 18)	14	In 01 (In 17)
2	In 03 (In 19)	15	+5V switched
3	In 04 (In 20)	16	AGND
4	In 05 (In 21)	17	AGND
5	In 06 (In 22)	18	AGND
6	In 07 (In 23)	19	AGND
7	In 08 (In 24)	20	AGND
8	In 09 (In 25)	21	AGND
9	In 10 (In 26)	22	AGND
10	In 11 (In 27)	23	AGND
11	In 12 (In 28)	24	In 16 (In 32)
12	In 13 (In 29)	25	In 15 (In 31)
13	In 14 (In 30)		

I/O port — One DB25 female, front panel.

1	24 V return	14	+ 24 VDC out
2	Chassis	15	Analog out 3
3	Analog in 1 +	16	Analog in 1 -
4	Digital out 1	17	Digital out 2
5	Analog in 2 +	18	Analog in 2 -
6	Analog in 3 +	19	Analog out 1
7	Analog in 3 -	20	Analog 2 out
8	Analog in 4 -	21	+ 5 VDC out
9	Ground	22	Digital out 3
10	Digital out 4	23	Analog in 4 +
11	Digital in 4	24	Digital in 3
12	Digital in 2	25	Digital in 1
13	Ground		

Connectors (continued)

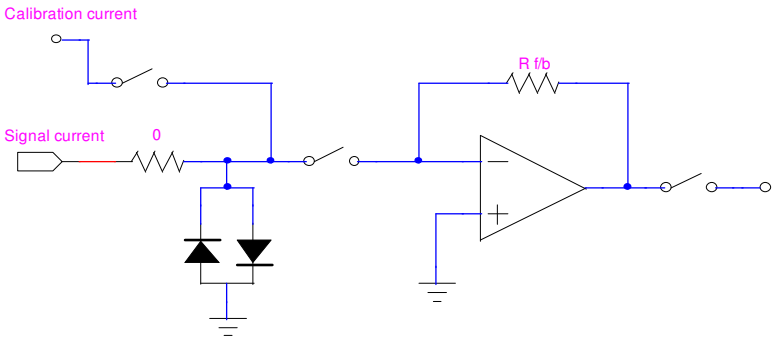
<table>
<tr><td>Digital I/O (Actuator)</td><td>DB9 female, front panel.
<table>
<tr><td>1</td><td>+24 V relay switched</td><td>6</td><td>+5V FET switched</td></tr>
<tr><td>2</td><td>24 V return</td><td>7</td><td>Opto In B</td></tr>
<tr><td>3</td><td>+5 V relay switched</td><td>+</td><td>+24 VDC out</td></tr>
<tr><td>4</td><td>+24 VDC out</td><td>9</td><td>Ground</td></tr>
<tr><td>5</td><td>Opto in A</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>High voltage out</td><td>SHV, front panel</td></tr>
<tr><td>High voltage in</td><td>SHV, front panel</td></tr>
<tr><td>Gate in</td><td>Lemo 00 coaxial, rear panel</td></tr>
<tr><td>Gate output</td><td>Lemo 00 coaxial, rear panel</td></tr>
<tr><td>Ethernet</td><td>RJ-45 jack, isolated</td></tr>
<tr><td>RS-232 / 485</td><td>Six pin mini-DIN (“PS/2”), isolated
<table>
<tr><td>1</td><td>Tx / RS-485 Tx-</td><td>4</td><td>Mode select (future option)</td></tr>
<tr><td>2</td><td>Rx / RS-485 Rx+</td><td>5</td><td>RS-485 Tx+</td></tr>
<tr><td>3</td><td>Gnd isolated</td><td>6</td><td>RS-485 Rx-</td></tr>
</table></td></tr>
<tr><td>Fiber optics</td><td>Two transmitter / receiver pairs for loop communications.

Two individual transmitters, HFBR ST bayonet for digital signaling.

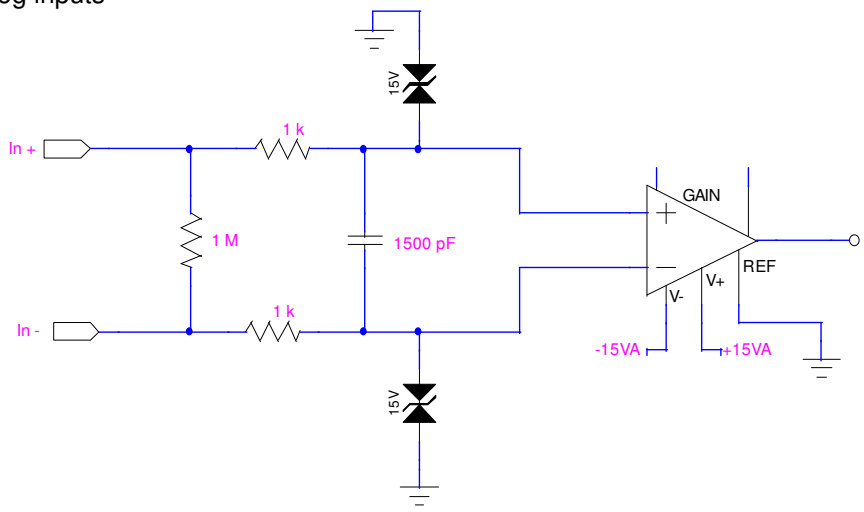
Avago HFBR ST bayonet connectors (compatible with 1 mm POF and 200 µm HCS fiber)</td></tr>
<tr><td>Power in</td><td>Lemo Redel PXG two-pin locking connector.
<table>
<tr><td>1</td><td>+24 VDC in</td></tr>
<tr><td>2</td><td>24 VDC return</td></tr>
</table></td></tr>
<tr><td>Ground</td><td>M4 threaded stud</td></tr>
</table>

Input / output circuits

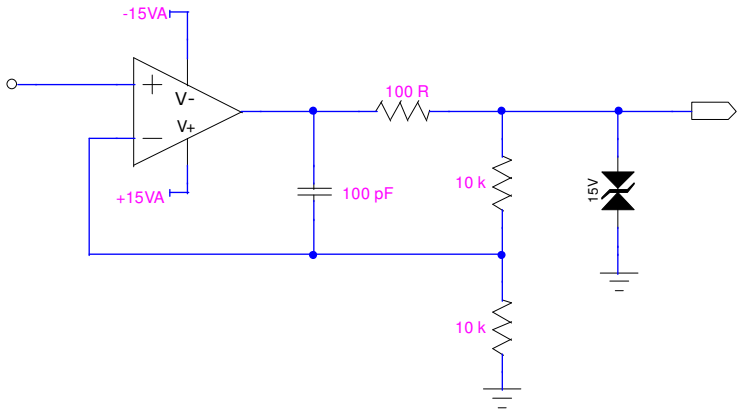
Current inputs



Analog inputs

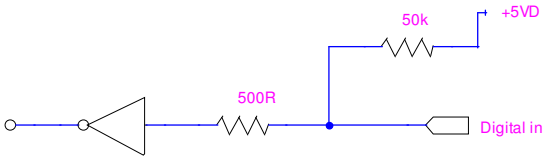


Analog outputs

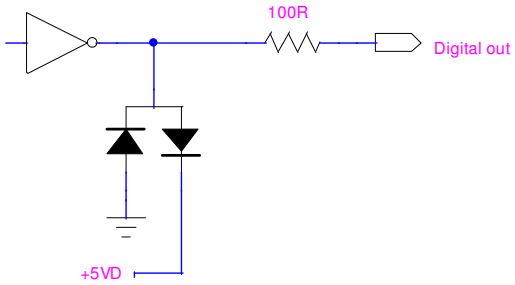


Input / output circuits (continued)

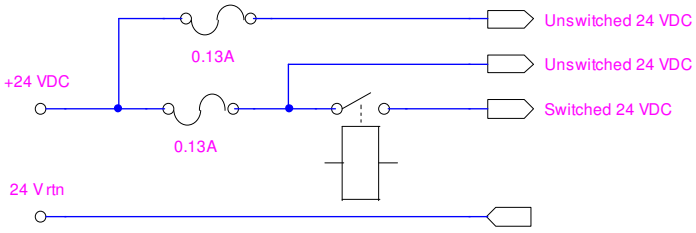
Digital inputs



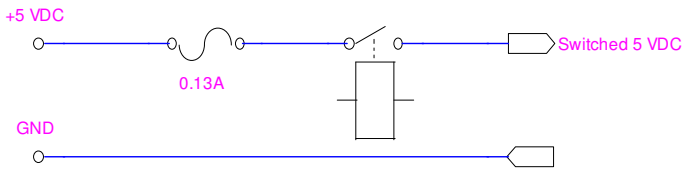
Digital outputs



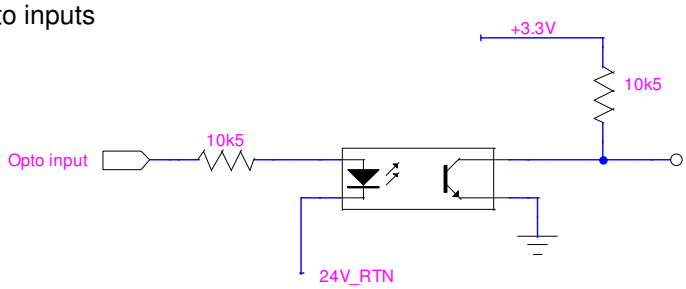
Actuator +24 VDC relay switched and un-switched

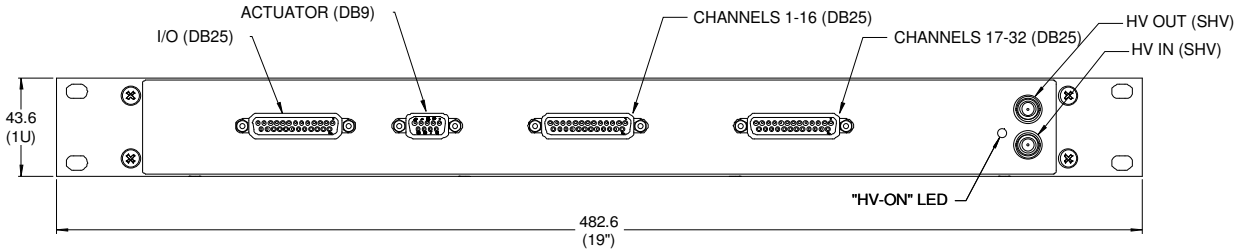


Actuator +5 VDC relay switched

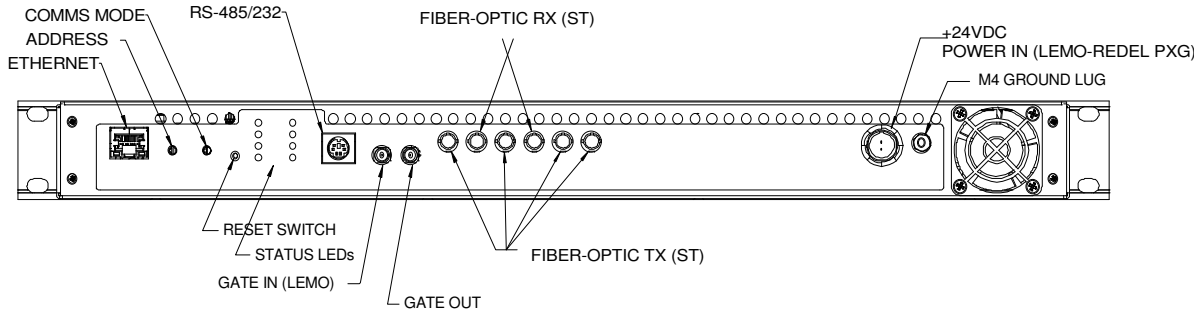


Opto inputs





FRONT VIEW



REAR VIEW
(ROTATED)

Dims mm

Ordering information

F3200E	F3200E thirty-two channel electrometer with user manuals, software, calibration data.
-XP20/10/5/2	Add HV supply positive 2000/1000/500/200 volts
-XN20/10/5/2	Add HV supply negative 2000/1000/500/200 volts
-RINx	Add current limiting series input resistor x ohm

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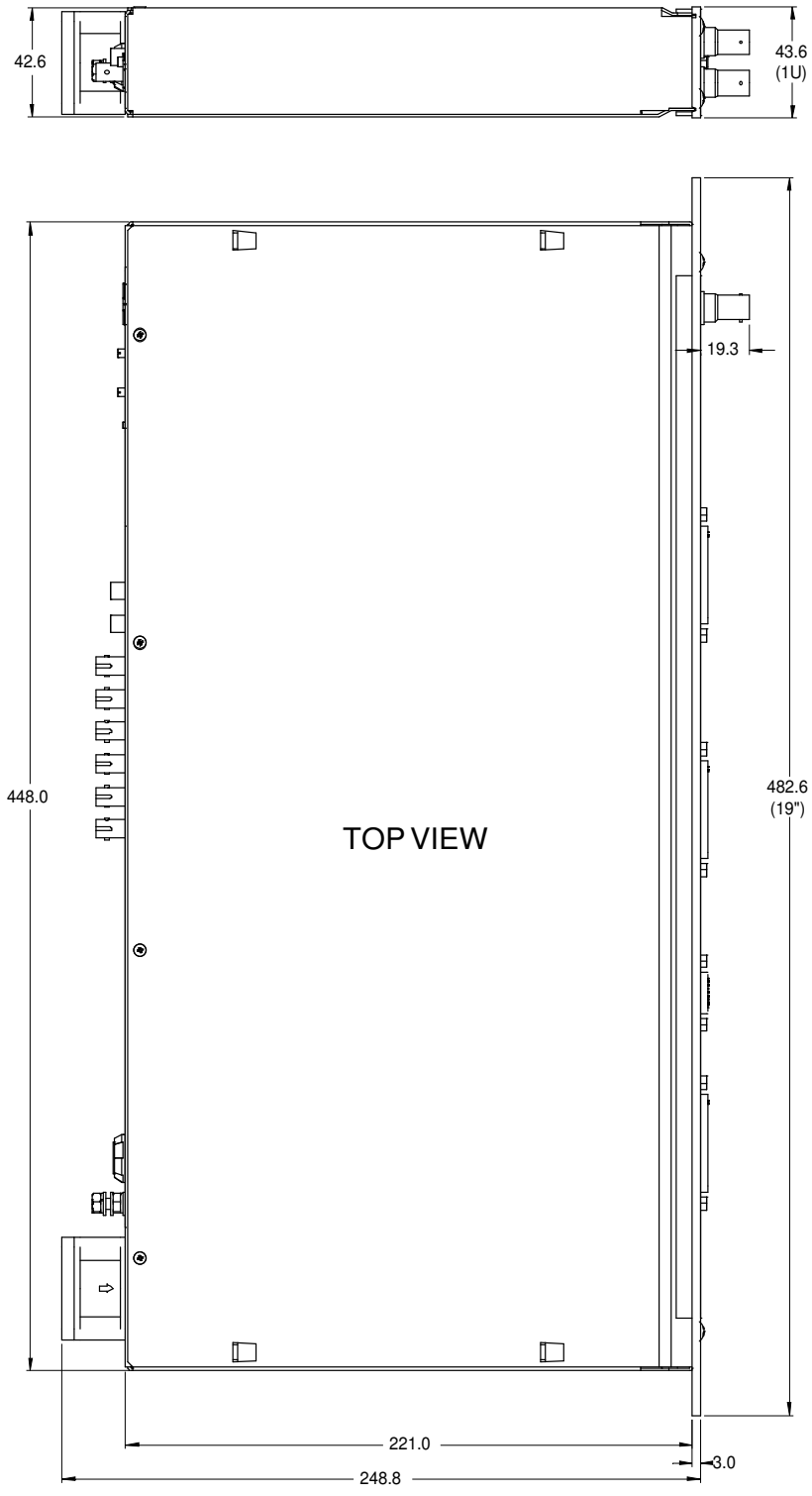

Dims mm